Intel's 300 mm Conversion

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INTRODUCTION

Large companies led previous wafer size conversions. These companies incurred the cost of conversion while leading the way for everyone else. Equipment suppliers and various consortia have led the 300 mm conversion. Tool suppliers have invested heavily to develop 300 mm tools and the efforts of several consortia contributed to the data collection efforts on many tool types. Early in the 300 mm equipment product development cycle, rigorous industry expectations were defined for tool performance, reliability, cost, utility consumption, installation design, environmental impacts, footprints, etc... Industry standards (SEMI) and guidelines (13001) were set for tool interfaces, wafer handling, buffering, automation, and safety. Many if not, most of the next generation tools are being developed on 300mm platforms.

THE ROLE OF CONSORTIA IN THE 300 MM WAFER SIZE CONVERSION

Intel and IBM led the past 150 mm and 200 mm wafer size conversions, respectively. Both companies did not realized any real benefit from leading the previous conversions as the disproportionate investment necessary to support development of each piece of equipment, necessary to equip a full pilot line, did not lead to any practical business advantage for the neither of the two companies. This was due to the following reasons. First, it still took many months from the development of equipment prototypes to the delivery of high volume manufacturing tools, thus eliminating any time advantage in converting to a larger wafer size. In fact, smaller wafers remained more cost effective for a long time even after the wafer size conversion had occurred.
Second, any other semiconductor company was able to purchase, with practically no time lag, the same equipment developed by the conversion leader without having invested in a costly equipment development.

Based on these negative experiences, it became clear in 1995 that no company was planning on coming forward and leading the 300 mm wafer size conversion and some form of consortium was the only alternative approach left for the industry in order to make progress in this important cost reduction program. In addition, due to the globalization of the equipment companies and also due to the extensive number of alliances, joint ventures and many other forms of cooperation among device manufacturers, it became clear to the Sematech companies that a new 300 mm consortium was necessary. This consortium had to focus on the evaluation of 300 mm equipment from any leading international equipment supplier. It had also to accept membership from any international device manufacturer who was interested in the 300 mm project. These considerations led to the formation of 13001 at the end of 1995. Almost simultaneously, the Selete consortium was formed in Japan with very similar objectives.

In 1996 and 1997, the burden of defining standards, equipment metrics and performing equipment testing resided almost exclusively with the consortia. Fortunately, from the very beginning 13001, Selete, J300, SEMI and the equipment supplier community at large agreed on a full cooperation. This agreement led to a very fruitful relation among these organizations that became very beneficial for the whole semiconductor industry. During these years Intel relied almost exclusively on the above consortia to carry on the 300 mm program. It was largely based on the high level of confidence in the data generated by 13001, and the other cooperating organizations, that the Intel decision to initiate internal activity on 300 mm was generated in 1998. Integration of the data generated by the consortia and data generated by Intel's evaluation teams resulted into a very easy task. It was from the positive assessment of this integrated equipment demonstration data pool that the decision to proceed with the 300 mm wafer size conversion was made at Intel in
1999.
Without the contribution of the consortia, it can be safely stated that, the 300 mm wafer size conversion would not be on in progress today. Tharik you to all those who participated in this effort!

TOOL PERFORMANCE

Assessment of good tool performance is critical when making a wafer size conversion. Good progress has been made in the non-die based tool (i.e. etcher, CVD) performance testing and footprint designs, which has counteracted some of the negative impacts from the die-based tools (litho expose equipment). The fact that upfront expectations were set with suppliers and were based on good industry consensus around tool performance, cost, and footprints is a key factor in enabling Intel's 300 mm program to move forward today. Additionally the standards that were adopted have enabled the industry to focus on common automation interfaces and will enable the 300 mm generation to be Intel's first fully automated factories.

Tool demonstrations at 13001 made solid contributions to increasing Intel's confidence level in the 300 mm toolset, assisting in our selection process, and processing test wafers. Between 70-80% of 13001 demonstrations were used as part of the selection process. The demo data that provided the most help was the reliability testing data. Roughly 40% of tools demonstrated at 13001 were selected by Intel for purchase counting selections completed to date. Intel's focus on 0.13 um technology and copper processing lead us to investigate many tools that were not part of the 13001 program.

STATUS

Intel is in the final stages of completing the tool selection process for the 0.13 um pilot line phase and has begun tool installation at our Dl C facility. Tools for use in test wafer generation and regeneration have been installed and are in the startup process.

One of Intel's biggest challenges has been in dealing with completely new tool installations and footprints, plus integrating these with the new automation systems. A fully mechanized factory supported by OHV requires very close attention to tool location relative to the overhead transport

system. Special templates have been used to ensure accuracy to +1- 10 mm at the loadport of the tool. Tool footprints are larger and bay widths are narrower than on the 200 mm generation, resulting in wider move in/out paths to reduce land locking.

The new automation systems for interbay and intrabay are being installed with the initial toolset and are in the process of startup. The first phase of the interbay system is now operational. The intrabay system is in the early testing stage. The new twenty-foot tall stockers are major architectural monuments that save storage space but require significant lay down space during installation.

Overall the new 300 mm factory is very different from a traditional factory in the sense that the tools are all new designs, footprints are larger, extensive automation and mechanization, and the overall size of the wafer carriers (FOUP's) drives the transition from hand delivery to mechanized transport of material.

SUMMARY

Intel decided to proceed with a formal 300 mm program in the middle of 1999 based on the progress that was made on equipment performance. This decision was cost driven as opposed to capacity. Additionally the focus for conversion has been on 0.13 um and copper processing. Since the decision to formally start the 300 mm program, significant progress has been made. The new 300mm factory has started the installation process and will continue throughout this year. Intel, upon successful completion of 300 mm wafer process development, would expect to begin the production ramp in 2002.

The early work that the industry put into preparing for the 300 mm conversion over the last several years gives us the opportunity to make this the most successful conversion ever.

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